What is claimed is:

1. A data compression read apparatus in a memory device, the apparatus comprising:
a first circuit that generates a first match signal when a predetermined bit position of each of a plurality of data words are a logical zero;
a second circuit that generates a second match signal when the predetermined bit position of each of the plurality of data words are a logical one; and
an output buffer circuit that either passes the predetermined bit or is in a high impedance state in response to the first or second match signals.

2. The apparatus of claim 1 wherein the first circuit comprises a first plurality of bit match circuits, each bit match circuit coupled to the predetermined bit position of each of the plurality of data words and the second circuit comprises a second plurality of bit match circuits, each bit match circuit coupled to the predetermined bit position of each of the plurality of data words.

3. The apparatus of claim 1 wherein the first circuit generates a logical true state when the predetermined bit position is a logical zero.

4. The apparatus of claim 1 wherein the second circuit generates a logical true state when the predetermined bit position is a logical one.

5. The apparatus of claim 1 and further including a logical OR operation coupled to the first and the second match signals such that the logical OR operation generates a match signal when one of the first or the second match signals is in a logical true state, the match signal coupled to and controlling a state of the output buffer circuit such that the output buffer circuit passes the predetermined bit when the match signal is true and places the output buffer circuit in the high impedance state when the match signal is false.

6. The apparatus of claim 1 wherein the memory device is a flash memory device.

7. A data compression read apparatus in a memory device, the apparatus comprising:

a first series of bit match circuits that generates a first match signal for indicating whether a predetermined bit position of each of a plurality of data words are a logical zero;

a second series of bit match circuits that generates a second match signal for indicating whether the predetermined bit position of each of the plurality of data words are a logical one; and

an output buffer circuit coupled to the first and second series of bit match circuits such that the output buffer outputs the predetermined bit when either the first or the second match signals indicate a true state and the output buffer being in a high impedance state in response to the first or second match signals indicating a false state.

8. The apparatus of claim 7 wherein the true state is a logical one and the false state is a logical zero.

9. The apparatus of claim 7 wherein each bit match circuit comprises:

a first transistor having an input connection, an output connection, and a first control gate;

a second transistor coupled in parallel to the first transistor, the second transistor having a second control gate;

a third transistor coupled between ground and the output connection, the third transistor having a third control gate; and

a control input circuit having an enable signal and the predetermined bit as inputs, the control input circuit generating a control signal output coupled to the first, second, and third control gates such that an input signal on the input connection is routed to the output connection when the control signal is in

one state and the output connection is grounded when the control signal is in a second state.

10. The apparatus of claim 9 wherein the first transistor is a p-channel transistor and the second transistor is an n-channel transistor.

11. The apparatus of claim 9 wherein the first state is a logic one and the second state is a logic zero.

12. A data compression read apparatus in a flash memory device, the apparatus comprising:

a first series of bit match circuits that generates a first match signal for indicating when a predetermined bit position of each of a plurality of data words are a logical zero;

a second series of bit match circuits that generates a second match signal for indicating when the predetermined bit position of each of the plurality of data words are a logical one;

a logical OR operation having inputs coupled to the first and second match signals, the logical OR operation generating a true indication when one of the first or second match signals indicates a true state and a false indication otherwise; and

an output buffer circuit coupled to the logical OR operation such that the output buffer passes the predetermined bit in response to the true indication and the output buffer being in a high impedance state in response to the false indication.

13. The apparatus of claim 12 wherein the logical OR operation comprises a logical OR gate.

14. A bit match circuit comprising:

a first transistor having an input connection, an output connection, and a first control gate;

a second transistor coupled in parallel to the first transistor, the second transistor having a second control gate;

a switching device coupled between ground and the output connection, the switching device having a control input; and

a control input circuit having an enable signal and a predetermined data bit as inputs, the control input circuit generating a control signal output coupled to the first and second control gates and the control input such that an input signal on the input connection is routed to the output connection when the control signal is in a first logical state and the output connection is grounded when the control signal is in an inverse logical state.

15. The circuit of claim 14 wherein the first logical state is a logical one and the inverse logical state is a logical zero.

16. The circuit of claim 14 wherein the first transistor and the switching device are n-channel transistors and the second transistor is a p-channel transistor.

17. The circuit of claim 14 wherein the predetermined data bit is a data bit from a data word involved in a compression operation in a memory device.

18. A method for performing a compressed read operation in a memory device having an output buffer, the method comprising:

performing a bit match operation on a data bit at a predetermined bit location of each word involved in the compressed read operation;

if the data bits in each of the predetermined bit location in each word are equal, enabling transfer of the data bit through the output buffer; and

if the data bits in each of the predetermined bit location in each word are not equal, indicating an error condition.

19. The method of claim 18 wherein the error condition is indicated by creating a high impedance condition in the output buffer.

20. A method for performing a compressed read operation in a memory device having an output buffer, the method comprising:

combining a first plurality of bit match circuits in series such that each bit match circuit is coupled to a predetermined bit location of a plurality of data words;

combining a second plurality of bit match circuits in series such that each bit match circuit is coupled to the predetermined bit location of the plurality of data words;

performing a logical zero bit match operation on a plurality of predetermined bits in the predetermined bit location with the first plurality of bit match circuits;

performing a logical one bit match operation on the plurality of predetermined bits with the second plurality of bit match circuits;

if the plurality of predetermined bits in each of the plurality of data words have a same value, enabling transfer of the value through the output buffer; and

if the plurality of predetermined bits in each of the plurality of data words do not have the same value, causing the output buffer to be in a high impedance state.

21. An electronic system comprising:

a processor that controls the operation of the electronic system; and

a memory device coupled to the processor, the memory device having a data compression read apparatus comprising:

a first circuit that generates a first match signal when a data bit in a predetermined bit position of each of a plurality of data words are a logical zero;

a second circuit that generates a second match signal when the data bit in the predetermined bit position of each of the plurality of data words are a logical one; and

an output buffer circuit that either passes the data bit or is in a high impedance state in response to the first or second match signals.

22. A data compression read apparatus in a memory device, the apparatus comprising:

a first series of bit match circuits that generates a first match signal for indicating when a predetermined bit position of each of a plurality of data words are a logical zero;

a second series of bit match circuits that generates a second match signal for indicating when the predetermined bit position of each of the plurality of data words are a logical one;

a plurality of propagation repeater circuits that regenerate the first and second match signals, a first propagation repeater circuit coupled between a predetermined number of the first series of bit match circuits and a second propagation repeater circuit coupled between a predetermined number of the second series of bit match circuits; and

an output buffer circuit coupled to the first and second series of bit match circuits such that the output buffer outputs the predetermined bit when either the first or the second match signals indicate a true state and the output buffer being in a high impedance state in response to the first or second match signals indicating a false state.

23. A method for performing a compressed read operation in a memory device having an output buffer, the method comprising:

performing a bit match operation on a data bit at a predetermined bit location of each word involved in the compressed read operation;

if the data bits in each of the predetermined bit location in each word are equal, enabling transfer of the data bit through the output buffer; and

if the data bits in each of the predetermined bit locations in each word are not equal, determining the predetermined bit location of the word that is causing an error condition.

24. The method of claim 23 wherein the predetermined bit location is determined by exiting the compressed read operation.

25. The method of claim 24 and further including repairing the error condition.

26. The method of claim 23 and further including repairing each word.